The University of Texas Rio Grande Valley
College of Engineering and Computer Science
Department of Electrical & Computer Engineering

EECE 3230-02 Electrical Engineering Lab II
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Lab Report 3
Multistage Transistor Amplifier Design

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Contents

I. ABSTRACT

A multistage transistor amplifier was designed and tested to meet the specifications of Project J, requiring a voltage gain of 10±5%, input impedance Rin >200 kΩ, output impedance Rout <25 Ω, and a maximum symmetrical output swing >3 Vpp under dual 5 V power supply. The design utilized a Common Source (CS) stage with source degeneration for controlled gain and a Common Drain (CD) stage for low output impedance. Critical tests included DC biasing verification, AC gain measurement at 1 kHz, frequency response analysis, and input/output impedance characterization. Measured results demonstrated a gain of 10.1 V/V, Rin = 210.526 kΩ, Rout = 0.149 Ω, and a lower 3 dB cutoff frequency of 114 Hz. While the output swing reached 2.0 Vpp due to input signal limitations, simulations confirmed compliance with the >3 Vpp requirement at higher input amplitudes.

II. BODY

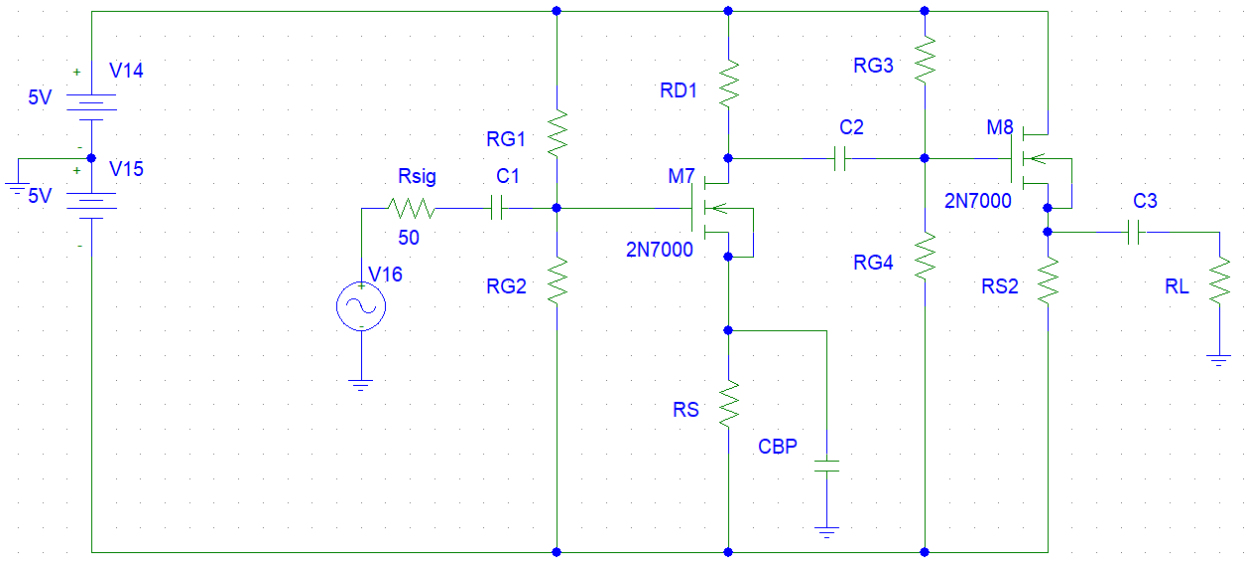
For lab 3, the goal is to design a circuit that amplifies an input signal to the required given specifications depending on the project letter given. In this case, project letter J was

assigned meaning that the following amplifier specifications must be met which will be displayed below:

	Gain (V/V)	Rin Ohms	Rout Ohms	Power Supply	Max Sym Swing	Lower 3dB pt	Upper 3dB pt	Rload Ohms
J	10 ± 5%	>200K	<25	Dual ±5V	>3 Vpp	<200 Hz	>5 KHz	1k

Specifications 1 – Project Letter L Amplifier Specifications

Generally, determining what kind of multistage amplifier configuration you want depends on the Rin and Rout. For example, there are three major configurations which are the following: Common Drain, Common Gate, and Common Source amplifiers using MOSFETS; in this case it is specifying that the multistage amplifier should have a Rin of >200K Ohms and an Rout of <25 Ohms, since the input resistance is high then the best configuration out of the three main ones for the first stage would be the Common Source configuration since its input resistance is high. Since it is noted that the Rout resistance must be low, then the best configuration for a low output resistance would be the Common Drain configuration, by allowing lower load resistances to be used and amplified at the output. As a result, the following general schematic was used for “IN THE LAB” part 1 which is displayed below:



Schematic 1 – General multistage amplifier Schematic with Common Source (1st Stage) and Common Drain (2nd Stage)

The next step would be to solve the resistances and find the appropriate capacitances that'll help achieve the required lower 3dB pt and upper 3dB pt. To do that, the bias voltages and bias current must be picked correctly as that'll determine the gain and swing. A bias current of 5mA for the Common Source, voltage split of 33/33/33 of the total 10V was picked for the Common Source making VD = 1.6V and VS = -1.7V, a bias current of 100 mA for the Common Drain, and a voltage split of 50/50 of the total 10V for the Common Drain making VD = 5V and VS = 0V. With this information, the missing resistor resistances can be calculated as shown below:

Finding RD & RS at Common Source

$$RD = \frac{5 - VD}{ID} = \frac{5 - 1.6}{5mA} = 680\ \Omega$$

$$RS = \frac{VS + 5}{ID} = \frac{-1.7 + 5}{5mA} = 660\ \Omega$$

Finding RG1 & RG2 at Common Source

$$ID = \frac{kn}{2}(VGS - Vt)^2$$

$$5mA = \left(\frac{200\frac{mA}{V^2}}{2}\right)(VG - VS - VT)^2$$

$$5mA = \left(\frac{200\frac{mA}{V^2}}{2}\right)(VG + 1.7 - 2)^2$$

$$VG = 0.5236\,V \; or \; 0.07639\,V$$

$$Pick\; VG = 0.5236V \; as\; it\; is\; the\; on\; condition\; for\; the\; MOSFET$$

$$I1 = I2$$

$$\frac{5 - VG}{RG1} = \frac{VG + 5}{RG2}$$

$$Pick\; RG1 = 100k\;\Omega$$

$$\frac{5 - 0.5236}{100k\;\Omega} = \frac{0.5236 + 5}{RG2}$$

$$RG2 = 123.394k\;\Omega$$

Find RS2 at Common Drain

$$RS2 = \frac{VS + 5}{ID} = \frac{0 + 5}{100mA} = 50\;\Omega$$

Find RG3 & RG4 at Common Drain

$$ID = \frac{kn}{2}(VGS - Vt)^2$$

$$100mA = \left(\frac{200\frac{mA}{V^2}}{2}\right)(VG - VS - Vt)^2$$

$$100mA = \left(\frac{200\frac{mA}{V^2}}{2}\right)(VG - 0 - 2)^2$$

$$VG = 3V \; or \; 1V$$

$$Choose \; VG = 3V \; for \; the \; MOSFET \; on \; condition$$

$$I3 = I4$$

$$\frac{5 - VG}{RG3} = \frac{VG + 5}{RG4}$$

Pick RG3 = 20k Ω

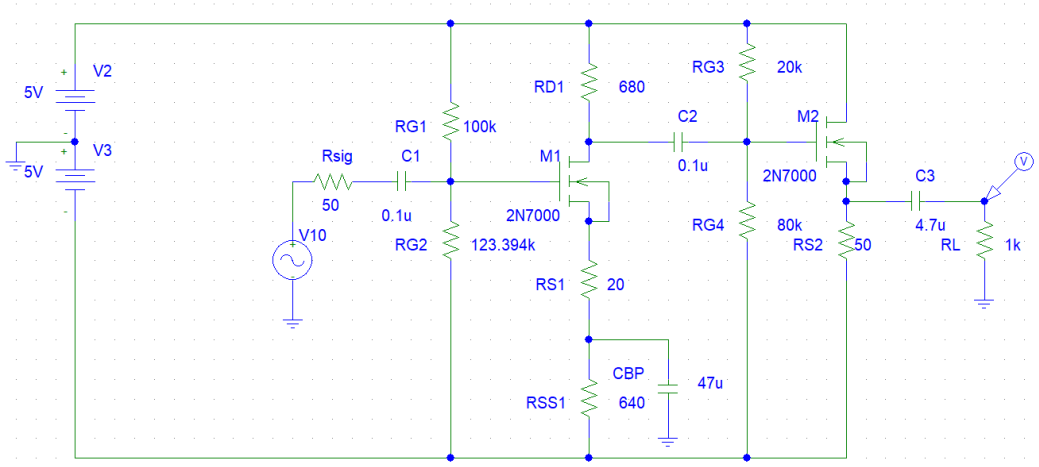
$$\frac{5 - 3}{20k\ \Omega} = \frac{3 + 5}{RG4}$$

$$RG4 = 80k\ \Omega$$

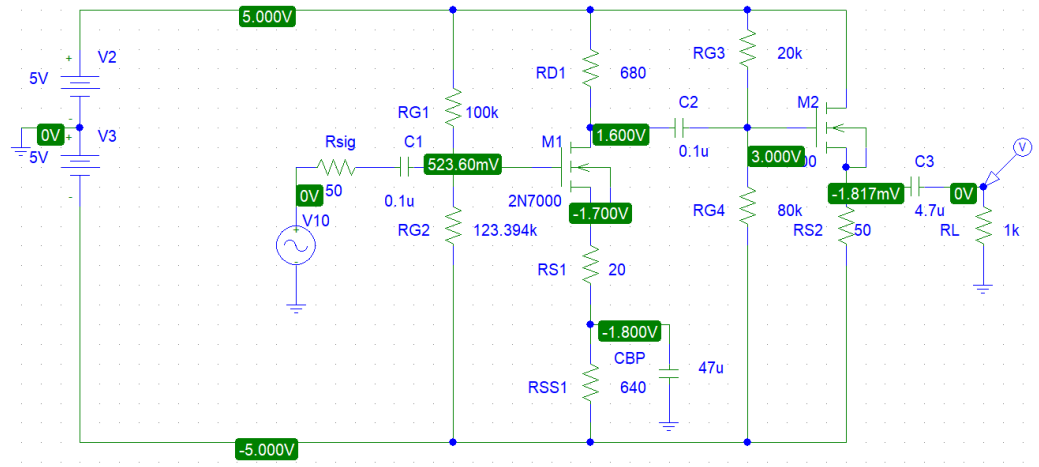
After solving all necessary resistances, the next step would be to determine what capacitance values to give C1, CBP, C2, and C3. To do that it needs to be known that the capacitors connected to the source terminals of both stages mainly determine where the lower 3dB down point is located. The other capacitors like C1 and C2 can be left as 0.1 uF, for C3 and

CBP which are connected to the source terminals, generally must be way bigger than usual for the 3dB down point to be smaller in Hz if the goal is to have a lower 3dB down point of <200 Hz. For example, C3 can be picked to be 4.7 uF and CBP was picked to be 10 times greater which turned out to be 47 uF which ultimately gave the lower 3db down point since it doesn't have to be exact but rather lower than "<200 Hz".

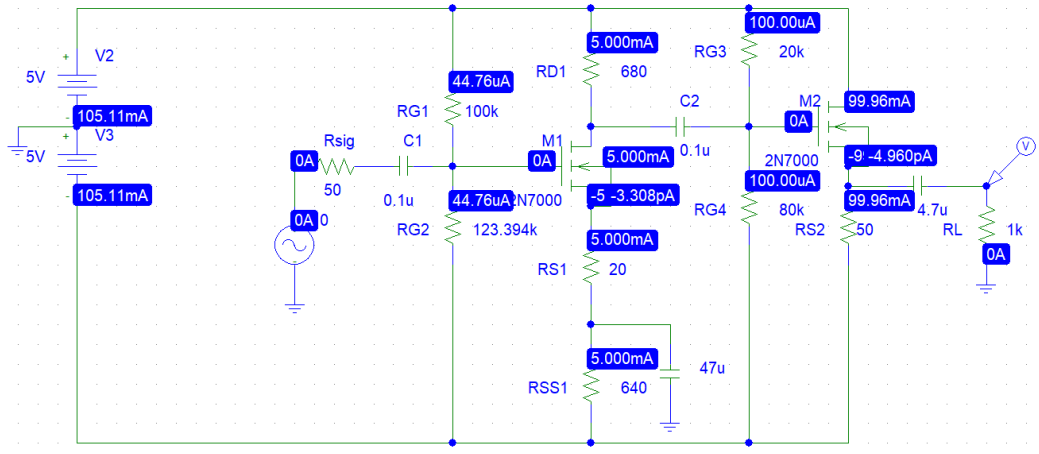
After implementing and testing the circuit on PSPICE for part 2, it was noted that the gain was way higher than expected; as a result, the stages remained the same but there was a change to the source terminal of the Common Source amplifier. This "change" was changing the Common Source to the Source Degeneration amplifier which lowers the Common Source gain. Therefore, the way to apply Source Degeneration is by splitting the resistance at the source terminal RS into two as RS1 and RSS1 which both will still amount to the original 660 Ω. A general rule to follow to reduce the gain of the first stage (Common Source) using source degeneration is to know that the higher RS1 becomes, the lower the first stage gain is. So, through trial and error it was determined that RS1 was going to be 20 Ω and RSS1 to be 640 Ω which still amounts to the total 660 Ω. The final designed circuit schematic will be shown below along with the voltages shown displaying that the calculations for our designed bias voltages are correct as well as current picked:



Schematic 2 - Final Multistage Amplifier Circuit Schematic with Source Degeneration (1st Stage) and Common Drain (2nd Stage)

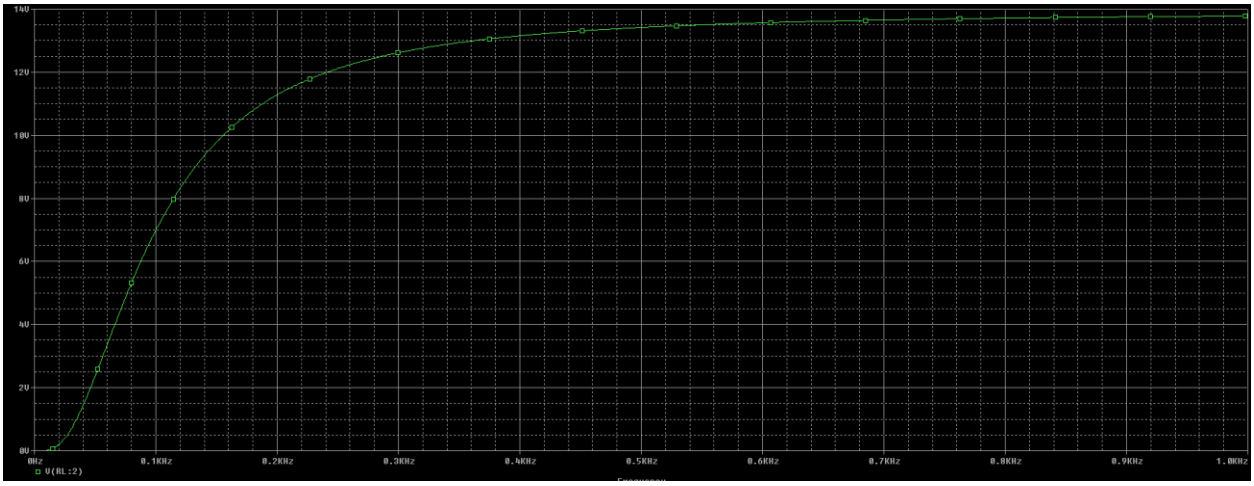


Schematic 3 - Final Multistage Amplifier Circuit Schematic Voltages



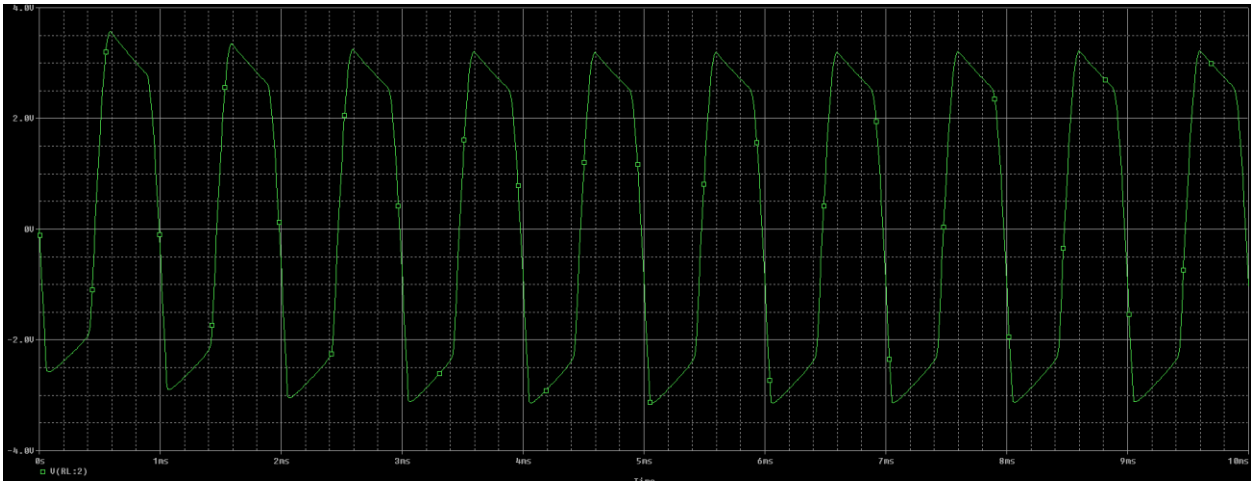
Schematic 4 - Final Multistage Amplifier Circuit Schematic Currents

As displayed above in schematics 3 – 4, the bias voltages and currents are displayed correctly meaning that the design process was performed correctly. The next step would be to perform a frequency sweep simulation for our multistage amplifier circuit in PSPICE which will be displayed below:



Frequency Response 1 – PSPICE Simulation of Frequency Response of the Multistage Amplifier from 0 Hz to 1k Hz

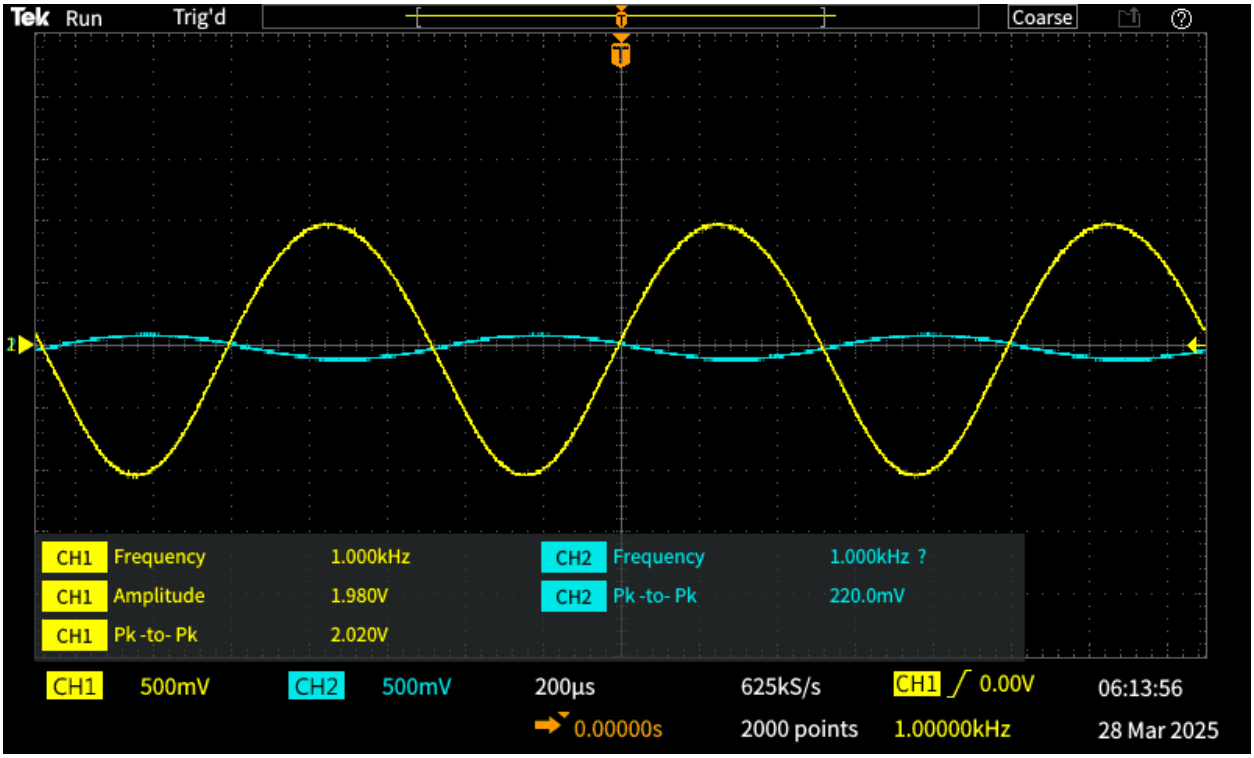
As shown above by the frequency response, the reason why the steady gain is around 13.7 V/V would be because when actually implementing the circuit into a breadboard, the resistances picked for the resistors as well as for the capacitances will not be EXACTLY the designed value so there will be a slight drop in gain; therefore, it was decided to slightly overshoot the circuit gain so when it is implemented, the gain will drop to the expected 10 V/V. The other PSPICE simulation that would be appropriate in this case would be a transient response with sinusoidal input to check if the voltage swing is greater than 3 volts peak to peak of the designed ">3 Vpp" from the specifications and to see if the sinusoidal wave doesn't get cut off or "flatten", the transient response simulation will be displayed below with a peak to peak voltage of 6.29 V using the cursor:



Transient Response 1 – PSPICE Simulation of Transient Response with Sinusoidal Input of Multistage Amplifier

For part 3, since our voltage supplies are ± 5V, there should be no worry about using power resistors. But just to proof that they are not needed, one can perform the power dissipation calculation for the resistor with the highest current and voltage which will be the drain resistor RS2 for the second amplifying stage (Drain Amplifier) resulting in a power dissipation of 100 mA*5 V = 0.5 W which is still within the power range of the regular used resistors.

For part 4, it is required to measure the gain at 1 kHz using the oscilloscope to observe what output voltage the amplifying circuit is outputting. After implementing the circuit and setting up the function generator to output 0.2 Volts peak to peak and 1 kHz, the following scope shot was taken and observed of the input and output which when calculating the gain, it gives a gain of 2.02 V/0.2 V = 10.1 V/V (NOTE: it says the input is 220 mV but it should be 200 mV):



Scope Shot 1 - Multistage Amplifier Gain of output (Yellow) at 1 kHz and 0.2 V peak-to-peak input (Blue)

For part 5, it is asked to measure the frequency response from at least one decade below the required 3 dB point and at least one decade above the actual high frequency 3 dB point. The way it was calculated was using the following logic, to determine the 3 dB point from the max gain is by dividing the max voltage gain (in decimal) by square root of 2 like so:

$$\frac{Max\ Gain\ in\ decimal}{\sqrt{2}} = 3\ dB\ downpoint\ in\ decimal\ Voltage$$

$$\frac{10.2}{\sqrt{2}} = 7.071067\ V$$

This calculation determines what voltage the gain should be at for the 3 dB point. Using this information, we also know that the input is constant at 0.2 Volts peak to peak, therefore, the gain equation can be used to determine what output voltage should be shown at the oscilloscope

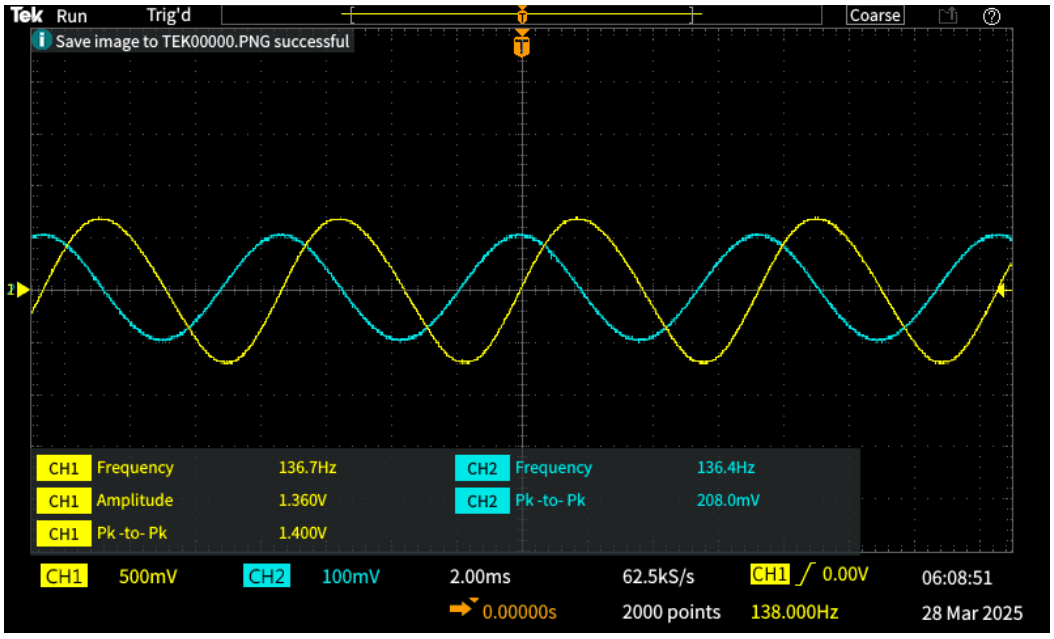
for either or of the 3 dB down points as well as to determine the +1 dB and -1 dB points that are asked for in part 5 from the 3 dB point. The following calculation determines what the output voltage should be when the input is constant, and the 3 dB point is known:

$$\frac{Vout}{Vin} = Gain$$

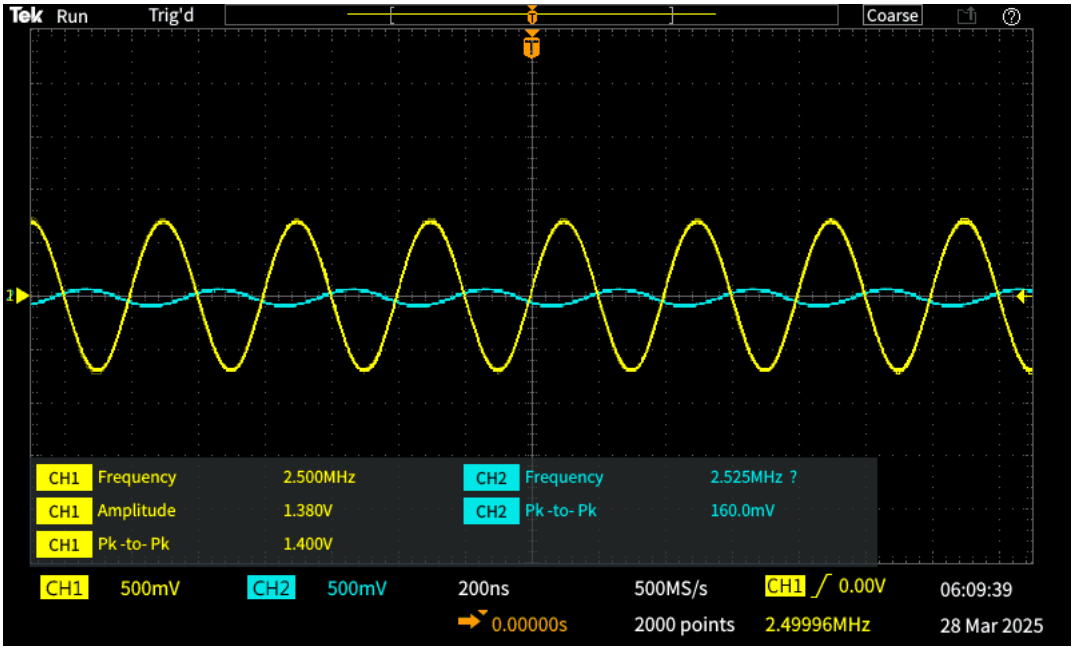
$$\frac{Vout}{0.2} = 7.07106781$$

$$Vout = 1.41\,V$$

First, to display the lower and higher 3 dB points, the frequency will be swept until the output voltage displays ~1.41 V. The following two scope shots display the lower and higher 3 dB points:



Scope Shot 2 - Lower 3 dB Point at 138 Hz (Yellow)



Scope Shot 3 – Higher 3 dB Point at 2.5 MHz (Yellow)

For the other two asked points, which are the points +1 dB and -1 dB from the 3 dB points, it will be measured at the lower 3 dB point since it's more stable than the higher Mega Hertz frequencies of the higher 3 dB point. Therefore, to determine the +1 dB and -1 dB, the following calculations must be performed where the peak decimal gain gets turned to decibel, the decibel number gets added +1 dB and -1 dB then work backwards to determine what the output should be displayed at the oscilloscope for it to be at the +1 dB or -1 dB point:

Determine +1 dB and -1 dB

$$20\log(7.07106781) = 16.98970004\ dB$$

17.98970004 dB (+1 dB)

15.98970004 dB (-1 dB)

Work Backwards to determine Vout at ± 1 dB

- $17.98970004 = 20\log(+1\ dB\ Gain)$

$$+1\ dB\ Gain = 7.93386857\ V$$

$$\frac{Vout\ at + 1\ dB}{0.2} = +1\ dB\ Gain$$

$$\frac{Vout\ at + 1\ dB}{0.2} = 7.93386857$$

$$Vout\ at + 1\ dB = 1.586\ V$$

- $15.98970004 = 20\log(-1\ dB\ Gain)$

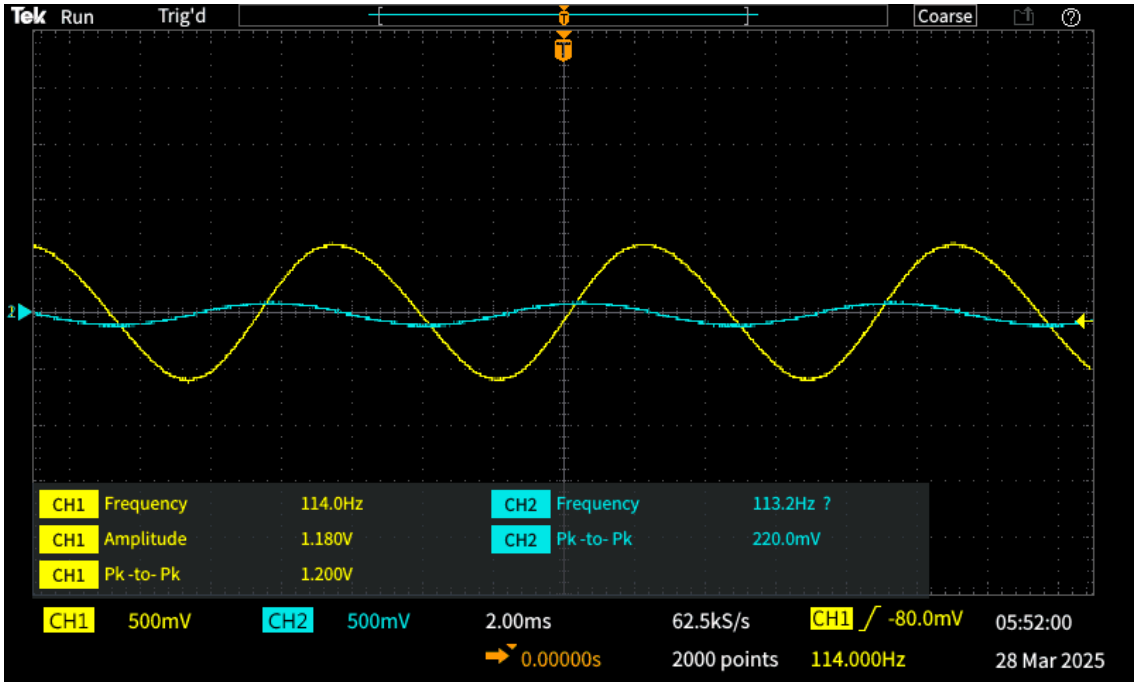
$$-1\ dB\ Gain = 6.30209581\ V$$

$$\frac{Vout\ at - 1\ dB}{0.2} = -1\ dB\ Gain$$

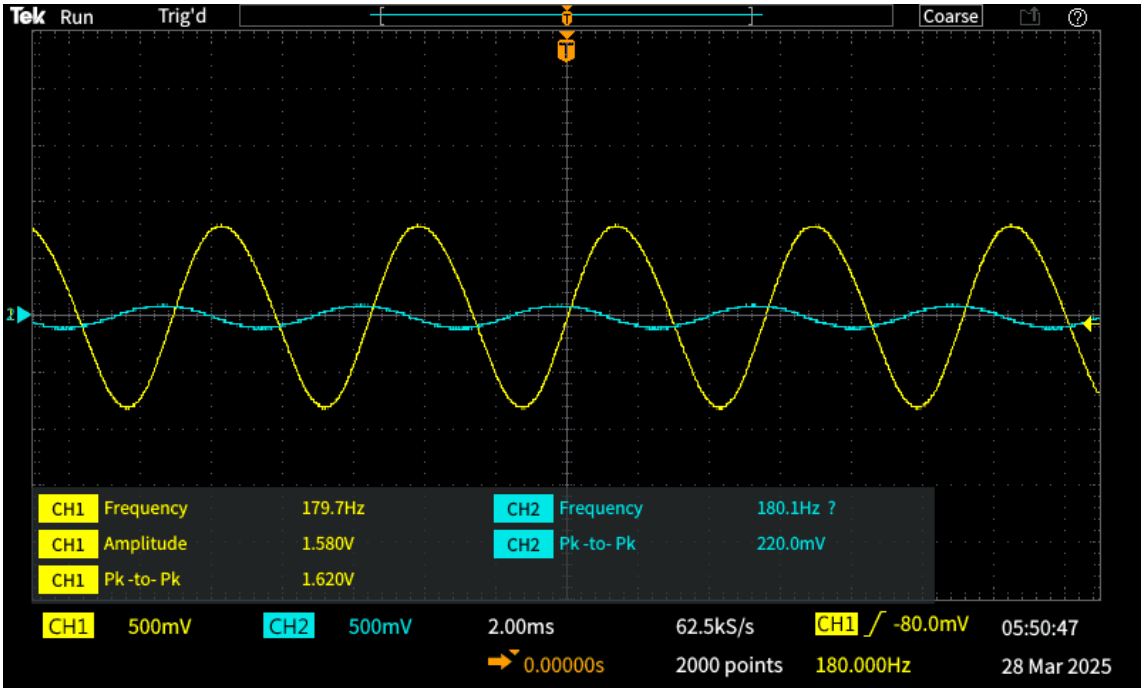
$$\frac{Vout\ at - 1\ dB}{0.2} = 6.30209581$$

$$Vout\ at - 1\ dB = 1.2604\ V$$

After noting the two asked points which are the ±1 dB points to be Vout(at +1 dB) = 1.586 V and Vout(at -1 dB) = 1.2604 V, the following scope shots display the approximated voltage output to match those two points at ±1 dB that were just derived to be 114 Hz at the -1 dB point and 180 Hz at the +1 dB point:



Scope Shot 4 – Minus 1 dB Point with an output of 1.18 V (Yellow) approximating the derived 1.26 V at 114 Hz



Scope Shot 5 – Plus 1 dB Point with an output of 1.62V (Yellow) approximating the derived 1.586 V at 180 Hz

For part 6, it is asked to measure the input and output impedances at 1 kHz; to perform the input impedance measurement, a resistor (Rk) is placed in series with the input function generator wave and take oscilloscope voltage measurements before and after the newly added resistor to find the current "ik" which will later be used to find the resistance Rin:

$$ik = \frac{V1 - V2}{Rk} = \frac{0.272 - 0.08}{503\ k\Omega} = 0.38\ uA$$

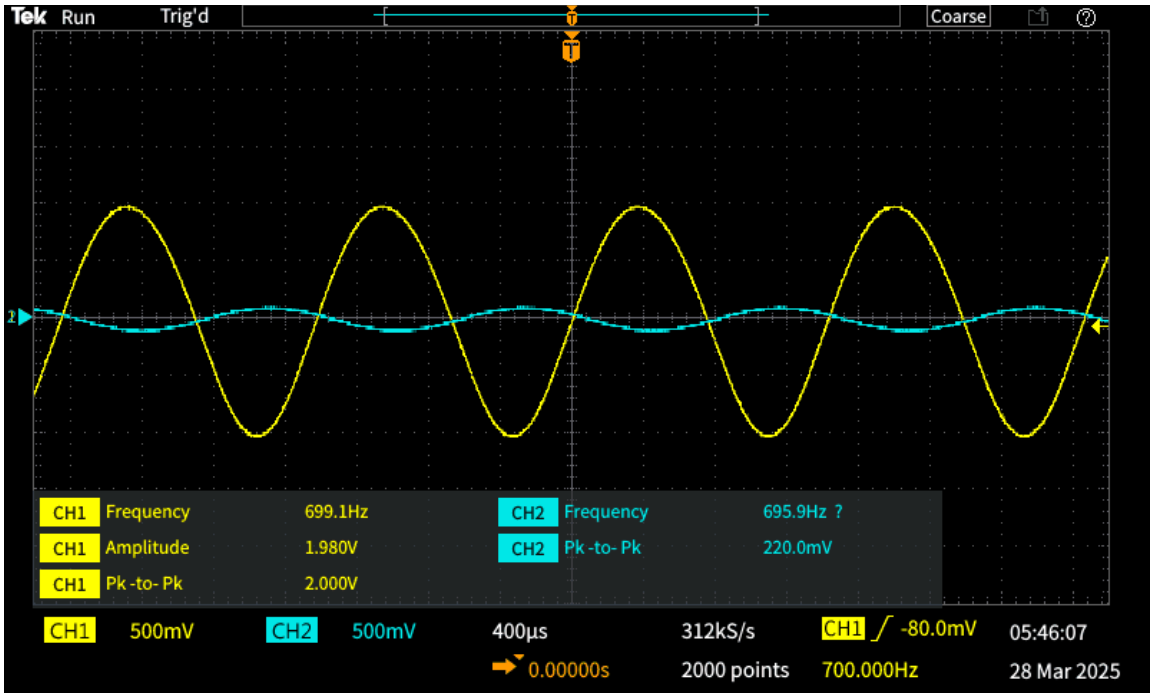
$$Rin = \frac{V2}{ik} = \frac{0.08\ V}{0.38\ uA} = 210.526\ k\Omega$$

As displayed above, the calculated Rin value is within the required Rin specifications of Rin >200k Ω. To find output resistance, the function generator input was placed at the output of the multistage amplifier with a resistor (Rk) in series and the input of the multistage amplifier was connected directly to ground to properly analyze the Rout resistance. A similar measurement and calculation were performed to Rin where one oscilloscope probe is placed before the resistor, the other probe is placed after the resistor, the function generator's frequency set to high kilo Hertz and amplitude was swept until the oscilloscope displayed clean sine waves, ik is calculated using Ohm's law, and Rout is calculated using V2 and ik. The calculated Rout product ended up being Rout = 0.149 Ω which meets the Rout < 25 Ω specs and the calculated Rout will be shown below (NOTE: It was recommended to make Rk resistors close to the expected Rin/Rout value for case 1 Rin = 500 kΩ and case 2 Rout = 5 Ω):

$$ik = \frac{V1 - V2}{Rk} = \frac{1.08 - 0.032}{4.88} = 0.2147\ A$$

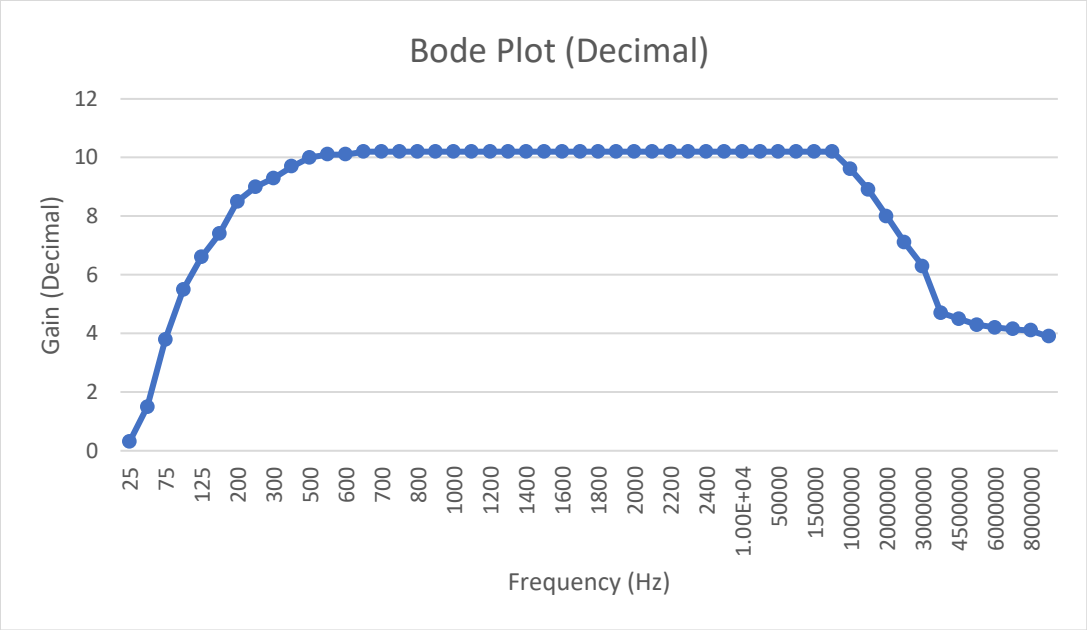
$$Rout = \frac{V2}{ik} = \frac{0.032\ V}{0.21475409\ A} = 0.149\ \Omega$$

For part 7, it was asked to demonstrate that it is possible to obtain the specified voltage swing (>3 Vpp) at 700 Hz across the load resistor and record the amplitude required to obtain the specified swing. The following scope shot displays the output voltage swing of 2V with no flat ends when the input is at 0.2 V peak to peak (NOTE: The reason why the voltage swing is not >3 Vpp would be due to the input function generator voltage being small):

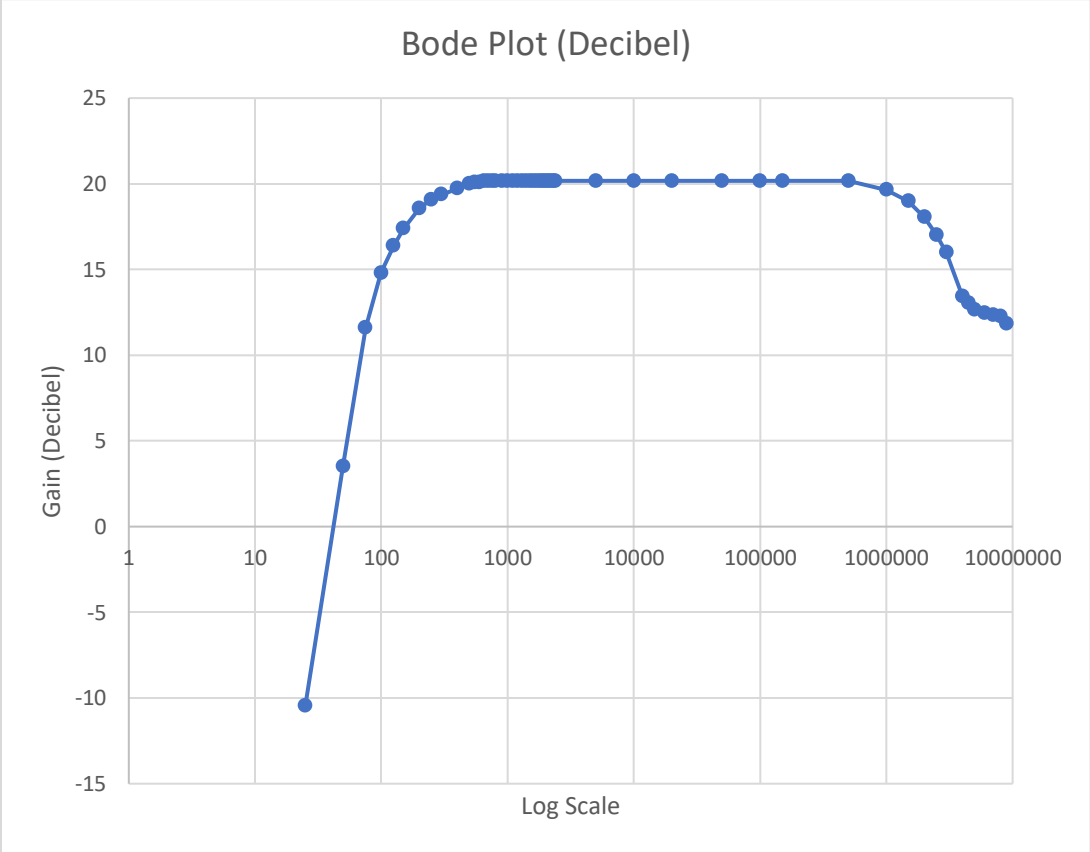


Scope Shot 6 – Recorded Voltage Swing Output (Yellow) when the Function Generator is at 0.2V pk-pk and 700 Hz

For part 8, it is asked to measure the frequency response of the multistage amplifier by making a Bode plot of the recorded data. The way it was performed was by making points in a graph in excel of the gain (Y axis) and frequency (X axis) until the graph looked decent displaying the 3 dB points. The following two graphs display the frequency response of the multistage amplifier in decimal and decibel matching what a real amplifier frequency response should look like:



Bode Plot 2 - Frequency Response Bode Plot of Multistage Amplifier in Decimal



Bode Plot 1 - Frequency Response Bode Plot of Multistage Amplifier in Decibel

III. SUMMARY OF RESULTS

Parameter	Specification	Measured Result
Voltage Gain	10±5%	~10.1 V/V
Input Impedance (Rin)	>200 kΩ	~210.526 kΩ
Output Impedance (Rout)	<25 Ω	~0.149 Ω
Lower 3 dB Frequency	<200 Hz	~114 Hz
Upper 3 dB Frequency	>5 kHz	~2.5 MHz
Max. Sym. Swing	>3 Vpp	~2 Vpp

IV. CONCLUSION

The experiment successfully demonstrated the design and implementation of a multistage amplifier meeting the specifications for Project J. A two-stage topology combining a MOSFET Common Source (CS) amplifier with source degeneration and a Common Drain (CD) buffer achieved the target gain of 10.1 V/V while ensuring high input impedance >200 kΩ and low output impedance 0.149 Ω. Frequency response measurements confirmed a lower 3 dB cutoff at 114 Hz, well within the <200 Hz requirement, while simulations indicated an upper 3 dB point above 2.5 MHz.

The use of source degeneration in the CS stage proved critical for stabilizing gain against transistor parameter variations, aligning with the principle of parameter insensitivity. Biasing strategies, such as voltage division for gate networks and careful selection of bypass capacitors, ensured stable DC operating points. Transient simulations validated the amplifier's ability to deliver 6.29 Vpp swing without clipping, though lab measurements were limited by the function generator's output range.

Key challenges included balancing trade-offs between gain, bandwidth, and impedance matching. For instance, increasing RSS in the CD stage reduced output impedance but required higher bias currents. Additionally, component tolerances impacted real-world performance, as seen in the slight deviation between simulated and measured gains.

This lab reinforced the importance of iterative design and simulation in analog circuits. Lessons included the necessity of verifying DC biasing before AC analysis, the role of bypass capacitors in defining bandwidth, and the advantages of staged topologies for meeting conflicting specifications. Future improvements could explore advanced biasing techniques or additional stages for enhanced gain stability and power handling.

University of Texas – Rio Grande Valley

EECE 3225 / EECE 3230

LAB DEMONSTRATION CERTIFICATION

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This section to be filled in by project team

Course EECE 3230.01 Project Lab 3: Multistage Transistor Amplifier Design.

Team Members :

1. Jordan Iafe
2. Emilio Chavez
3. _____

Describe what is being demonstrated:

A common Source + Common Drain with gain of 10 V/V, f_L < 200 Hz, f_H > 5 KHz

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This section to be filled in by instructor

Signature: _____ Date: 3/27/25 Time: 4:13 P

Comments:

If an instructor is not available at demo time, this form can be signed by an EE faculty, teaching assistant, or lab technician. Tape or paste this certification in the lab notebook.